REMARKS

Claims 1 – 20 were pending in the application. Claims 5 and 15 have been cancelled. Claims 1, 6, 12, 13, and 16 have been amended. Accordingly, claims 1-4, 6-14, and 16-20 are pending in the application.

Double Patenting

In the Office Action of November 28, 2005, claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 5 of copending Application No. 10/136,619. Applicant has filed a terminal disclaimer in compliance with 37 CFR 1.321(c) to overcome this rejection.

35 U.S.C. § 102 Rejections

In the present Office Action, claims 1-4, 7-10, and 12-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hagersten, US 5,864,671 (hereinafter "Hagersten '671"). Applicant has amended the claims to clarify the nature of the invention. Applicant submits each of the pending claims recite features which are neither taught nor suggested by the cited art, either singly or in combination. Accordingly, Applicant requests reconsideration in view of the present amendments and the following comments.

Applicant submits that all of the claimed limitations recited in claim 1 are not disclosed or suggested by the cited art. For example, claim 1 as amended recites:

"A multiprocessing system comprising:
a plurality of processing subsystems, each including a cache memory;
a memory subsystem including a directory;
a network interconnecting said plurality of processing subsystems and said memory subsystem;
wherein the network includes **a mode unit separate from the processing subsystems and the memory subsystem, wherein the network is configured to:**
receive a given coherency request initiated by a requesting processing subsystem, wherein the coherency request is

not visible to other processing subsystems or the memory subsystem; and

control whether the given coherency request is transmitted through said network according to a directory protocol or a broadcast protocol; and

wherein an encoding of said given coherency request excludes an indication of whether said given coherence request is to be transmitted according to said directory protocol or said broadcast protocol; and

wherein **when said coherency request is transmitted through said network according to said directory protocol, said given coherency request is transmitted through said network to said memory subsystem.**"

It is noted that the mode unit is separate from any of the processing subsystems and the memory subsystem. It is further noted that the mode unit is configured to receive coherency requests that are not visible to other processing subsystems or the memory subsystem and, when the coherency request is transmitted through the network according to a directory protocol, transmit the coherency request to the memory subsystem. Since the directory is included in the memory subsystem, it should be clear that the mode unit and the directory are different and perform different functions.

In contrast, Hagersten '671 discloses

"In accordance with one aspect of the present invention, there is provided a hybrid protocol for permitting the home node of a requested memory block to take advantage of a directory cache hit. Utilizing the information contained in the cache's directory entry, a memory access request may be rapidly serviced in the manner associated with the aforementioned directory protocol.

In the event of a directory cache miss, i.e., there is not a directory entry that corresponds to the requested memory block in the directory cache, a directory-less protocol is advantageously employed. As the name implies, the directory-less protocol permits the home node to service a memory access request from any node in the network without employing information that is typically provided in a directory entry associated with the directory protocol." (Hagersten '671, col. 11, lines 10-25)

Hagersten '671 describes a hybrid protocol, wherein a memory access request may be serviced according to a directory protocol or a directory-less protocol. The determination of which protocol to use is made by the home node consulting a directory cache. The home node is one of the nodes of the network that includes memory that stores the requested memory block. It is not separate from the memory. Furthermore, if there is a cache hit, the home node does not transmit the request to another node that stores the requested block, since the home node already stores the requested block. Applicant finds no teaching or suggestion in Hagersten '671 of a mode unit separate from the processing subsystems and the memory subsystem and configured to: receive a given coherency request initiated by a requesting processing subsystem and not visible to other processing subsystems or the memory subsystem. Further, Applicant finds no teaching or suggestion in Hagersten '671 that when the mode unit transmits a coherency request through the network according to a directory protocol, the given coherency request is transmitted through the network to the memory subsystem. Accordingly, Applicant submits that claim 1 is patentably distinguishable from Hagersten '671. Further, as each of the remaining independent claims 12, 13, and 16 include features similar to that of claim 1, each of the remaining independent claims is believed patentably distinguishable from the cited art for similar reasons. As each of the dependent claims includes at least the features of the above independent claim upon which it depends, each of the dependent claims is believed patentable as well.

In the present Office Action, claims 1-7 and 13-17 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Martin, US 2002/0133674 A1 (hereinafter "Martin"). Applicant submits each of the pending claims recite features which are neither taught nor suggested by the cited art, either singly or in combination. Accordingly, Applicant requests reconsideration in view of the present amendments and the following comments.

Regarding prior claims 1, 7, 13, and 16 the Examiner asserts in paragraph 24 that Martin teaches:

> "A coherency mode unit (26, Fig. 1) configured to store an indication (42, Fig. 4; see also Pg. 3, Par. 57) to control whether a given coherency request is transmitted through said network according to a directory protocol or a broadcast

protocol (Pg. 3, Par. 52). (While Martin does not name this unit a coherency mode storage unit, the cache controller he discloses performs the function of the mode unit disclosed by the instant application.)"

Applicant submits that all of the claimed limitations recited in amended claim 1 are not taught by the cited art. For example, as noted above, claim 1 as amended recites:

"A multiprocessing system comprising:
a plurality of processing subsystems, each including a cache memory;
a memory subsystem including a directory;
a network interconnecting said plurality of processing subsystems and said memory subsystem;
wherein the network includes **a mode unit separate from the processing subsystems and the memory subsystem, wherein the network is configured to:**
receive a given coherency request initiated by a requesting processing subsystem, wherein the given coherency request is not visible to other processing subsystems or the memory subsystem; and
control whether the given coherency request is transmitted through said network according to a directory protocol or a broadcast protocol; and
wherein an encoding of said given coherency request excludes an indication of whether said given coherence request is to be transmitted according to said directory protocol or said broadcast protocol; and
wherein when said coherency request is transmitted through said network according to said directory protocol, said given coherency request is transmitted through said network to said memory subsystem."

As previously noted, the mode unit is separate from the processing subsystems and the memory subsystem. The mode unit is also configured to receive a given coherency request initiated by a requesting processing subsystem and not visible to other processing subsystems or the memory subsystem. These features are absent from Martin.

Martin discloses (e.g., see Figure 1) processor units 12a-12f, each of which includes a cache controller. Martin teaches that

"the cache controller 26 implements a state machine 29 that may execute either a snooping mechanism 30 or a directory mechanism 32. This state machine provides for a switch 34 whose state selects between these mechanisms ... the

state of the switch 34 is determined by monitoring the message traffic on the ordered request network 28." (Martin, para. 52-53).

However, Martin also teaches that the cache controllers are part of processor units 12a-12f, rather than being separate from the processing units. Applicant finds no teaching or suggestion in Martin of a mode unit separate from the processing subsystems and the memory subsystem. Accordingly, for at least this reason, claim 1 is patentably distinguishable from the cited art.

In addition, Martin discloses

"when a snooping mechanism is used for the transmission of cache coherence messages, for example, from a processor unit 12a, the cache coherence message is **duplicated and broadcast over the ordered request network** 28 to **each of the remaining processor units** 12b through 12f **and the memory controller** 11 of the shared memory system ...

Alternatively, referring to FIG. 3, when a directory mechanism is used for the transmission of cache coherence messages, the processor unit 12a **dual-casts the cache coherence message (arrow 27) to itself and the directory 21** which identifies those processor units, for example, processor units 12c and 12d (or the memory systems 16 itself) having the desired block 19 (e.g. as an owner or sharer of the block 19)." (Martin, para. 50-51).

Therefore, Martin teaches two mechanisms for processing cache coherence messages. A snooping mechanism broadcasts messages on a common bus such that each cache coherence request is visible to all other clients on the bus. A directory mechanism dual-casts the cache coherence message to the originating processor unit and the directory. It is noted that the directory resides on the memory node and is distinct from the cache controller. Consequently, both mechanisms make the cache coherence message visible to more than just the cache controller. Applicant finds no teaching or suggestion in Martin of a "mode unit configured to receive a given coherency request initiated by a requesting processing subsystem and not visible to other processing subsystems or the memory subsystem." For at least this reason as well, claim 1 is patentably distinguishable from the cited art. Further, as independent claims 13 and 16 include features similar to that of claim 1, independent claims 13 and 16 are believed patentably distinguishable from the cited art for similar reasons. As each of dependent claims 2-4, 6-11, 14,

and 17-20 includes at least the features of the above independent claim upon which it depends, each of dependent claims 2-4, 6-11, 14, and 17-20 is believed patentable as well.

35 U.S.C. § 103 Rejections

In addition, claims 8-10, 12, and 18-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Martin in view of U.S. Patent No. 5,887,138 ("Hagersten '138"). Applicant submits that claim 12, as amended recites features that are neither taught nor suggested by the cited art, either singly or in combination. Accordingly, Applicant requests reconsideration in view of the present amendments and the following comments.

A *prima facie* case of obviousness requires that the proposed combination teach or suggest all of the claimed limitations of the invention. Regarding prior claim 12, the Examiner states in paragraph 48 that Martin discloses:

> "A coherency mode unit (26, Fig. 1) configured to control whether a given coherency request is transmitted through said network according to a directory protocol or a broadcast protocol (Pg. 3, Par. 52). (While Martin does not name this unit a coherency mode storage unit, the cache controller he discloses performs the function of the mode unit disclosed by the instant application.)"

This portion of the rejection is similar to the 35 U.S.C. § 102 rejection of claim 1 as being unpatentable over Martin. Furthermore, claim 12 recites features similar to those of claim 1. Accordingly, for reasons similar to those presented above, claim 12 is believed patentably distinguishable from Martin. Since these features are also not found in Hagersten '138, Applicant submits that claim 12 is patentable over the cited art, either singly or in combination.

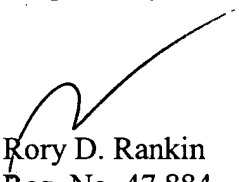
Also, claim 11 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Martin in view of Higuchi et al, US 5,774,731. In view of the above discussion, and the fact that dependent claim 11 includes at least the features of the independent claim 1 upon which it depend, further traversal of this rejection is believed unnecessary at this time.

CONCLUSION

In light of the foregoing remarks, Applicant submits that all pending claims are now in condition for allowance, and an early notice to that effect is earnestly solicited. If a phone interview would speed allowance of any pending claims, such is requested at the Examiner's convenience.

No fees are believed necessary; however, the Commissioner is authorized to charge any fees, which may be required to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account Number 501505/5181-99401/RDR.

Respectfully submitted,



Rory D. Rankin
Reg. No. 47,884
Attorney for Applicant(s)

MEYERTONS, HOOD, KIVLIN,
KOWERT & GOETZEL, P.C.
P. O. Box 398
Austin, Texas 78767-0398
(512) 853-8800

Date: March 14, 2006